

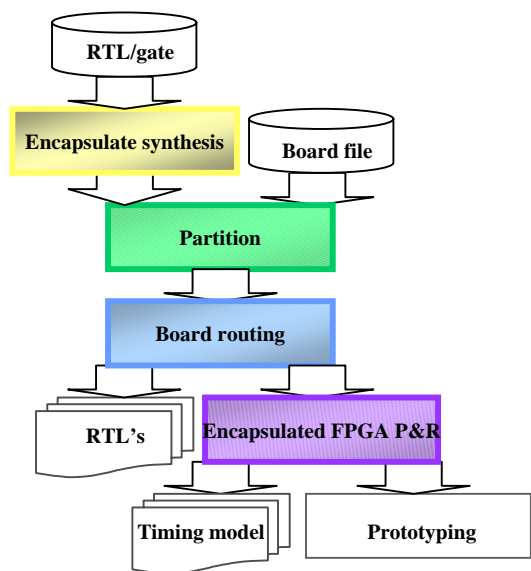
Overview

Mapping today's complex SoC designs into multiple-FPGA prototypes faces the challenge of finding a partition solution that

- (1) meets the constraints of the target hardware such as FPGA capacity, the clock distribution and limited connectivity in-between FPGA's.
- (2) is timing-correct.

The solution

ACE Compiler, with its hierarchical domain-driven technology, produces solutions which not only efficiently map big designs into the target hardware, but also run at the top performance.



ACE Compiler flow

The design is imported modularly with the encapsulated synthesis using any commercial FPGA synthesis tool. The successive partition step breaks the design into multiple FPGA's while honoring the board constraints. The board routing then assigns inter-FPGA signals to traces and consequently fixes the FPGA pin locations. The encapsulated FPGA P&R generates the programming bit-streams and the system timing model.

RTL may be exported as the other option to run the post-partition simulation or 2nd synthesis to further optimize timing on individual FPGA's.

The process could be completely automatic, or could be done manually on portion of the design for reasons such as anticipation of future design changes, target system interface or preferred grouping and let ACE Compiler complete the rest.

Domain-driven partition

If the design has a large number of external clocks or internally-generated clocks, the clock distribution on the multiple-FPGA prototype has to be carefully planned to manage the clock skew.

ACE Compiler could limit the number of clock domains partitioned into each FPGA to guarantee sufficient clock buffers to drive every clock in the FPGA. The clock generation could be isolated by partition to minimize the skew on board.

If the prototyping hardware platform has the limited capacity to drive internally generated clocks, ACE Compiler could limit the number of clock generations partitioned into each FPGA.

Gated clocks will be automatically identified and converted after the approval from the user. The conversion could be cascaded and crossing hierarchies.

Pin multiplexing

ACE Compiler is able to insert pin multiplexing to relieve FPGA pin shortage. The correct timing could be achieved with the domain-based pin-multiplexing and the exclusion of the combinatorial pass-through signals. Pin-multiplexing IP's could be either custom designed or acquired from Auspy's OEM's.

Hierarchical approach

ACE Compiler adopts hierarchical algorithms on all its operations to manage the design complexities. The memory required to run ACE Compiler on any big designs is usually less than the memory required by FPGA P&R of a single FPGA. ACE Compiler has automatically partitioned a 40 million gate design in hours on a normal Linux workstation.

Automatic Board routing

If the design has highly connected partitions that requires more connections than the hardware platform supports, ACE Compiler is able to route through unused pins of an intermediate FPGA to complete the connections.

If the target hardware supports cabling of connectors to dynamically configure the board connectivity, ACE Compiler is able to honor the manual cabling or automatically cable to provide the needed connections.

If the design has more tri-state buses than the hardware platform supports, ACE Compiler implements each tri-state bus in an intermediate FPGA after routing the tri-state and enable signals from involved partitions to this FPGA.

Clocks will be assigned to low-skew wires automatically.

Probe

ACE Compiler brings out probes to FPGA pins. Three types of probes are supported :

- 1) Fixed probes - selected before partition and its pin requirement will be taken into account by partition.
- 2) Incremental probes - selected after partition and will be brought to unused FPGA pins.
- 3) Fast probes - selected after FPGA P&R and will be brought to unused FPGA pins with fast incremental FPGA P&R.

Features

- Automatic compilation.
- RTL, gate-level or mixed language.
- Tight integration with major commercial FPGA synthesis tools.
- Hierarchical approach to handle very large designs.
- Solution for complex clocks.
- Automatic creation of loop-back configurations for global clocks.
- Automatic replication of clock modules such as PLL's or DCM's.
- Automatic gated-clock conversion.
- Timing-correct pin multiplexing.
- Logic replication to reduce FPGA pins and bring up prototyping performance.
- Impact analysis assisting manual partition.
- Global logic trimming.
- Automatic or manual cabling.
- Easy setup for non-FPGA daughter-boards.
- No design modifications needed for prototyping.
- Probe insertion.
- Insertion of custom debugging or co-simulation logic.
- Parallel synthesis and FPGA P&R.
- Dynamic board reconfiguration.
- GUI or script execution.

Integration

The encapsulated synthesis is integrated with commercial synthesis tools from Mentor Graphics, Synopsys, Synplicity and Xilinx.

The encapsulated FPGA P&R is integrated with Xilinx and Altera P&R tools.

ACE Compiler supports FPGA's from the Xilinx Virtex/Virtex-II/Virtex4/Virtex5 families, and Altera Stratix/Stratix-II families.

Platform

Linux
Windows
Solaris