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For Immediate Release **News Release**

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Auspy Development Inc. Joins Mentor Graphics OpenDoor Program

Auspy's Multiple-FPGA Partitioning Platforms for ASIC Prototyping Support Mentor's Precision Synthesis

Cupertino, CA, April 24, 2007- Auspy Development Inc., a leading provider of specialized multiple-FPGA partitioning solutions, announced that it has joined Mentor Graphics® (NASDAQ: MENT) OpenDoor^{SM} partner program. The partnership facilitates the integration of Mentor Graphics Precision® Synthesis tool with the Auspy Partition System II (APSII) and Auspy Custom Emulator Compiler (ACE Compiler) products, to immediately benefit designers worldwide seeking to cost effectively automate and accelerate the implementation of ASIC prototypes on today's state-of-the-art FPGAs.

"The integration of Mentor Graphics Precision Synthesis with our FPGA partitioning tools sets a new standard for ASIC prototyping," said Nang-Ping Chen, Founder and CEO of Auspy Development Inc. "Precision Synthesis delivers high-quality of results and includes advanced synthesis technologies for ASIC prototyping applications. The growing numbers of Precision Synthesis users can now leverage Auspy's powerful timing-driven partitioning solutions for their large and most complex ASIC prototyping projects".

"We are pleased to welcome Auspy Development Inc. into the OpenDoor program," said Daniel Platzker, FPGA Synthesis Product Line Director, Design Creation and Synthesis Division, Mentor Graphics. "By combining the ease-of-use, vendor-independence, and productivity benefits of our products with the advanced features of Auspy's APSII and ACE Compiler products, this agreement expands the choices available to Precision Synthesis users. Mentor Graphics synthesis technology, used with Auspy's leading-edge multiple-FPGA partitioning solutions, will be an important factor for enhancing any ASIC prototyping environment."

APSII partitions designs in RTL or gate-level into multiple FPGA implementations. The innovative automatic partition algorithm produces timing-correct high-speed prototypes, delivering high-quality results with minimal inter-FPGA connections. The relationship between the original and partitioned design is hierarchically established to ease cross-referencing. This hierarchical approach allows the tool to rapidly manage very large designs. An embedded timing engine optimizes system timing by converting gated clocks, minimizing combinatorial paths through FPGAs, limiting the number of clock domains partitioned into each FPGA to ensure that every clock is driven by a global buffer, isolating clock generation to balance the system skew reaching every FPGA, replicating FPGA clock modules such as PLL/DCM, and multiplexing pins within the same clock domain. Various constraints, including manual grouping, hard macros or target system interface, are observed to achieve the working partition.

ACE Compiler (ACE) maps designs in gate-level or RTL onto customer-built or commercial prototyping platforms. Equipped with the same partition engine as APSII, ACE performs automatic system routing to connect inter-FPGA signals through board traces, fix FPGA pin locations and assign system I/Os to connector pins on the target prototyping platform. The proprietary routing algorithm minimizes signal delays while searching paths through FPGAs, programmable switches and connected cables. Cables could be manually or automatically

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connected between connectors to provide extra traces for inter-FPGA connections. ACE is fully customizable, and can overcome prototyping platform limits such as the distribution of local clocks or the implementation of bi-directional buses in a shortage of global wires.

In a business environment where companies are facing increasingly tighter project schedules, both tools have proven to save weeks or months of development time. With APSII and ACE, users no longer need to manually partition every module in the design, work diligently within the limits of the target prototyping platform, modify the design for the clock distribution, degrade the prototyping performance due to the excessive pin multiplexing or manually complete hundreds or thousands of connections on the target prototyping platform. Both tools are tightly integrated with commercial FPGA synthesis tools from Mentor Graphics, Synopsys, Synplicity and Xilinx, as well as with FPGA vendor place-and-route tools from Altera and Xilinx. FPGA devices supported include Xilinx Virtex, Virtex II, Virtex 4 and Virtex 5, as well as Altera Stratix and Stratix II. For more information and to download a datasheet, visit www.auspy.com

Precision Synthesis forms the centerpiece of the Mentor Graphics FPGA flow — the industry's most comprehensive vendor-independent solution for FPGA design. With advanced support for ASIC prototyping (support for DesignWare® libraries, SDC constraints, gated-clock handling, etc.) plus advanced implementation and optimization techniques such as automatic mapping and inferencing of dedicated DSP and RAM blocks, Precision Synthesis is uniquely suited to handle today’s high-end FPGAs. In addition, Precision Synthesis features an award-winning design analysis capability, allowing designers to cross-probe between multiple views as well as to perform interactive static timing for rapid "what-if" analyses. Precision Synthesis reduces design iterations and enables faster, more predictable completion of designs, while delivering high quality of results. More details at www.mentor.com/synthesis

Mentor Graphics OpenDoor is the industry's leading and longest standing program supporting the development of integrated world-class solutions. OpenDoor provides access to a diverse number of partner companies that offer well integrated, leading edge software solutions that complement the Mentor Graphics suite of tools in all aspects of the design process. Over 95 OpenDoor partner companies have agreed to develop and maintain commercial integrations, expanding the choices available to Mentor Graphics users in all design processes. Hundreds of EDA products now interoperate with Mentor Graphics tools for ESDA, Top-Down Design, PCB Layout and IC Design. Check out www.mentor.com/company/partner_programs/opendoor/index.cfm

About Auspy Development, Inc.

Auspy Development Inc. is an EDA company specializing in next-generation multiple-FPGA partitioning solutions that cost-effectively automate the implementation of ASIC prototypes. Auspy licenses its products to commercial prototyping platform vendors. More than 100 copies of software have been sold worldwide through OEM partners and used successfully to partition complex ASIC designs with up to 40 million gates. Auspy is very proud of its commitment to customers and partners, and sells and supports custom-built prototyping platforms together with its distributors Magellan of Taiwan and ED&C of South Korea. http://www.auspy.com

About Mentor Graphics

Mentor Graphics Corporation (NASDAQ: MENT) is a world leader in electronic hardware and software design solutions, providing products, consulting services and award-winning support for the world’s most successful electronics and semiconductor companies. Established in 1981, the company reported revenues over the last 12 months of about $800 million and employs approximately 4,250 people worldwide. Corporate headquarters are at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777, USA. World Wide Web site: http://www.mentor.com/.